REMARKS

Claims 2 and 6 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chen et al., U.S. Patent No. 5,940,456 ("Chen") in view of Jean-Claude, U.S. Patent No. 4,542,500 ("Jean-Claude") or Humphrey et al., U.S. Patent No. 6,396,853 ("Humphrey") and Okamoto et al., U.S. Patent No. 6,094,442 ("Okamoto"). Claims 4 and 5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Chen in view of Okamoto.

Applicant respectfully requests the rejections of claims 2 and 6 be withdrawn

Claims 2 and 6 are directed at a circuit for a reception part of an synchronous digital hierarchy (SDH) transmission system which comprises a clock synchronizer for, among other things, receiving plesiochronous signals through a plurality of input channels, the clock synchronizer including a plurality of buffer memories corresponding to the plurality of input channels. One of the stated goals of the present invention is to reduce the cost and expense related to the number of circuits used to receive or transmit plesiochronous signals (see "Description of the Prior Art" section, page 1, lines 26-28, of the specification). The circuits in claims 2 and 6 achieve this, among other ways, by using a clock synchronizer to receive a number of plesiochronous signals.

In contrast, Chen discloses the reception of a number of signals through a plurality of input channels by a plurality of multiplexers, 502-505. At no time are these signals received by the synchronous clock, 510, shown in Chen. The reception of the signals by a plurality of multiplexers teaches away from one of the goals of the present invention, which is to reduce the amount of circuitry involved in the reception and transmission of plesiochronous signals.

In addition, as the Examiner points out, Chen does not disclose a clock synchronizer which includes a plurality of buffer memories as in claims 2 and 6 of the present invention. To make up for this deficiency, the Examiner relies on the disclosure of Humphrey or Jean-Claude.

However, neither Chen, Humphrey, nor Jean-Claude, taken separately or in combination, disclose, teach or suggest a clock synchronizer which receives plesiochronous signals from a plurality of input channels and includes a plurality of buffer memories, as in claims 2 and 6 of the present invention.

In sum, claims 2 and 6 would not have been obvious to one of ordinary skill in the art upon reading the combined disclosures of Chen, Jean-Claude, Humphrey or Okamoto.

Accordingly, Applicant respectfully requests withdrawal of the present rejection and allowance of claims 2 and 6.

Applicant respectfully requests withdrawal of the rejections of claims 4 and 5

Claims 4 and 5 are directed at a circuit arrangement for an SDH transmission system which comprises a transmission multiplexer for transforming a transmitted synchronous signal into a plesiochronous signal and a desynchronizer for recovering the plesiosynchronous signal clocks of the plesiochronous signals and for issuing the plesiosynchronous signals to a plurality of output channels.

In contrast, Chen discloses a plurality of multiplexers 502-505. There is no disclosure, teaching or suggestion in Chen that the multiplexers 502-505 recover plesiochronous signal clocks of plesiochronous signals and issue plesiochronous signals to a plurality of output channels, as in claims 4 and 5 of the present invention.

Claim 5 of the present invention includes a transmission demultiplexer contained in the desynchronizer of claim 4. In contrast, Chen explicitly states that devices 502-505 are multiplexers, not demultiplexers, as in claim 5 of the present invention.

In sum, Chen does not disclose, teach or suggest a circuit arrangement for an SDH transmission system, where a transmission processing means is connected to a transmission demultiplexer contained in a desynchronizer, as in claim 5 of the present invention.

In addition, as the Office Action points out, Chen does not disclose, teach or suggest a transmission multiplexer with an output coupled to the transmission processing means. The Office Action relies on Okamoto to overcome this deficiency.

However, neither Chen nor Okamoto, taken separately or in combination, discloses, teaches or suggests a desynchronizer following a transmission processing means for recovery of plesiochronous signal clocks of the plesiochronous signals and the issuance of plesiochronous signals to a plurality of the output channels, as in claims 4 and 5, nor do they disclose, teach or suggest that a transmission processing means is connected to a transmission demultiplexer contained in a desynchronizer, as in claim 5 of the present invention.

In sum, the inventions claimed in claims 4 and 5 would not have been obvious to one of ordinary skill in the art upon reading the combined disclosures of Chen and Okamoto.

Accordingly, Applicants respectfully request withdrawal of the present rejection and allowance of claims 4 and 5.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John E. Curtin at the telephone number indicated below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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By _____

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